

PREVIEW ENGINE **SDRAM** CCD BURST MODE MODULE CCD COMPRESSION **SDRAM** CONTROLLER CONTROLLER NTSC/PAL **OSP ENCODER** DSP SUBSYSTEM ARM IMAGE BUFFERS USB **MEMORY** CORE

FIC 2

VLC

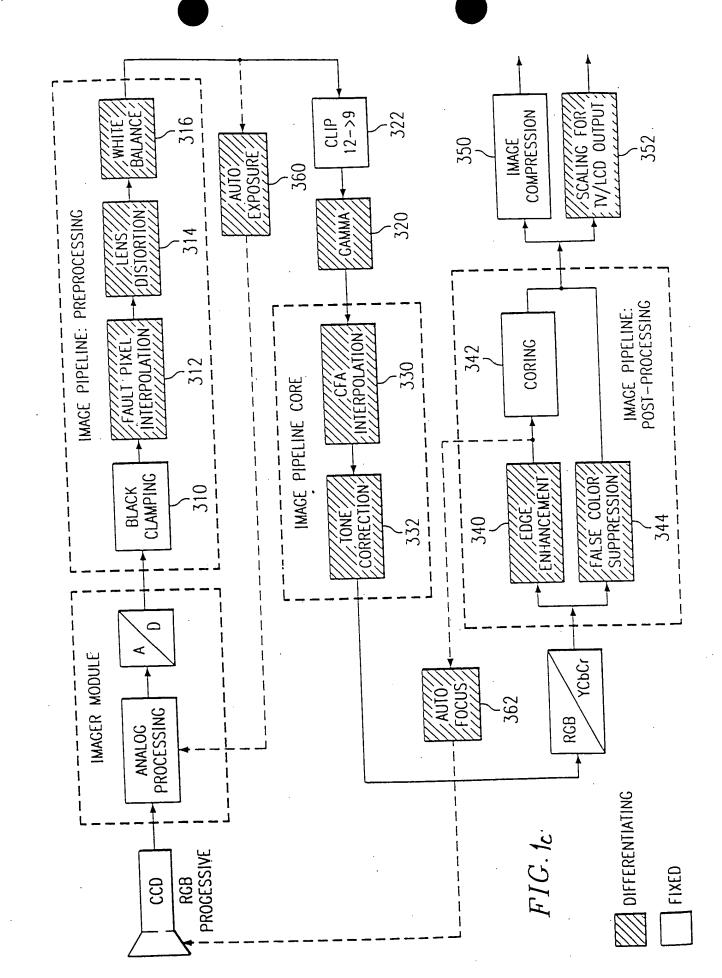
Maging

EXtension (iMX)

1/0

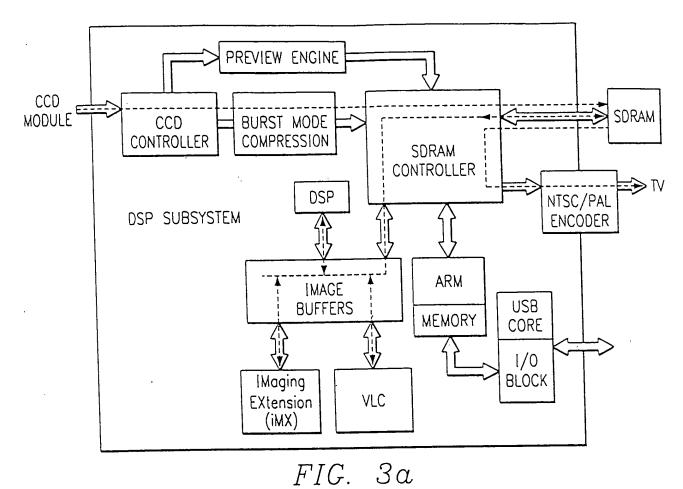
BLOCK

nesomete deser-



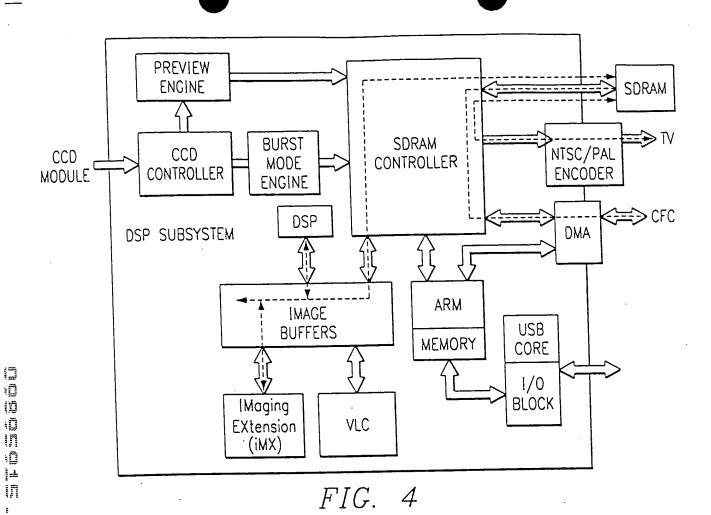
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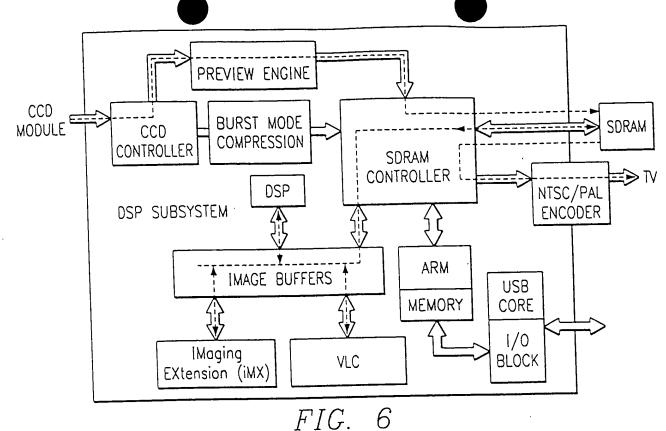
47.8 cyc/pxl =12230 cyc/16x16 pxl-**--** A **SDRAMC** $B \rightarrow B$ A -- A A --- A **OSP** $B \rightarrow B$ $A \longrightarrow A$ iMX**VLC** IMX USES BUFFER B IMX USES BUFFER A VLC, SDRAMC, DSP USE BUFFER B VLC, SDRAMC, DSP USE BUFFER A

FIG. 3b



PREVIEW ENGINE CCD **SDRAM** MODULE BURST MODE CCD CONTROLLER **COMPRESSION SDRAM** CONTROLLER DSP NTSC/PAL DSP SUBSYSTEM ENCÓDER ARM IMAGE **USB BUFFERS MEMORY** CORE 1/0 **BLOCK I**Maging **VLC EXtension** (iMX)

TIT



G	R	G
В	G	В
G	R	G
В	G	В
	B	B G G

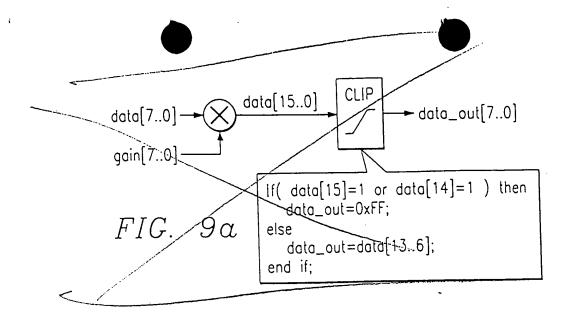
FIG. 7a

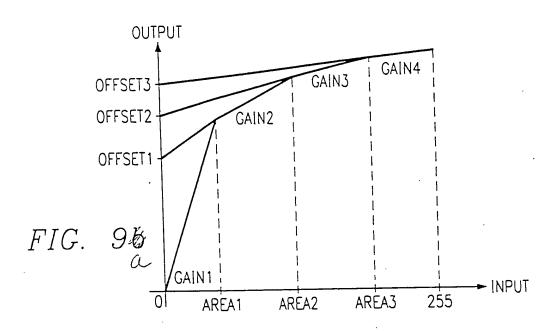
Ye	Су	Ye	Су
G	Mg	G	Mg
Ye	Су	Ye	Су
G	Mg	G	Mg

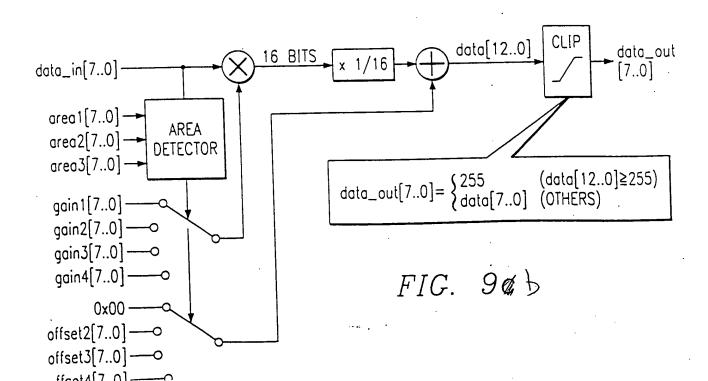
FIG. 7b

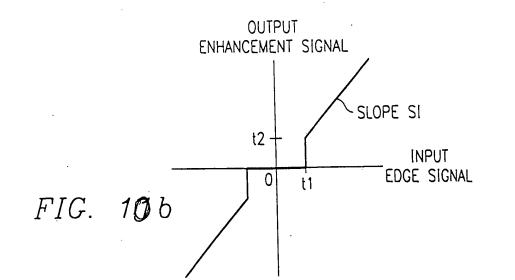
```
If (N[17]=1 \text{ or } N[16]=1 \text{ or } N[15]=1) then
      If (N[17]=1 \text{ or } N[16]=1) then
                                               OUT(7..0)=0xFF;
         OUT[9..0]=0x3FF;
                                            else
       else
                                               OUT[7..0] = IN[14..7];
         OUT[9..0]=IN[15..6];
                                             end if;
       end if;
   data[9..0]
                                                                            CLIP
                             CLIP
                                                                                      data_out
                                                                 18 BITS
                                                  18 BITS
                                   10 BITS
                  18 BITS
                                                                                      [7..0]
                                                   0x00010
PVGAIN[7..0]
                    gain 1 [7..0] — a
                                                white_balance_gain[7..0]
                    gain2[7..0]—
                    gain3[7..0] —
                     gain4[7..0]——
                                                 FIG. 8
              gain_selector_sw
```

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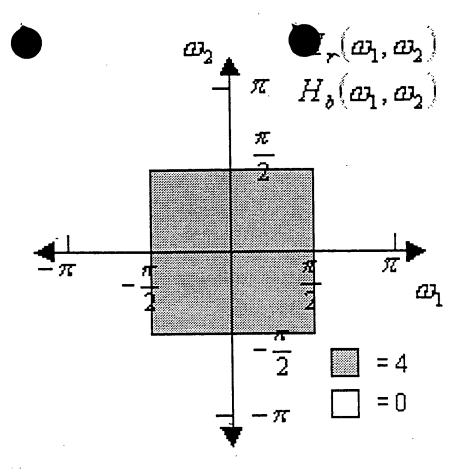
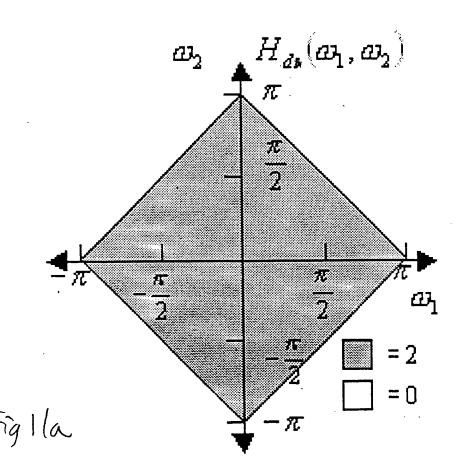


Fig.11b

(a) Ideal red/blue interpolation filter.



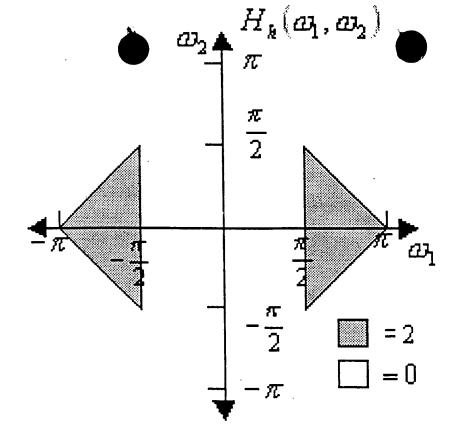


Fig. 11c
(a) Ideal horizontal high-pass filter.

